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A 2.56-µs Dynamic Range, 31.25-ps Resolution 2-D Vernier Digital-to-Time Converter (DTC) for Cell-Monitoring

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***Abstract*—Capacitive sensor array (CSA) has emerged as a prominent approach in the field of biomedical detection, particularly for the analysis of cell morphology and the construction of a Cell-on-CMOS platform. To enhance overall sensitivity, this paper presents a novel 2-D vernier digital-to-time converter (2D V-DTC) with a resolution of 31.25 ps and a dynamic range of 2.56 µs. The 2-D vernier structure attains sufficient resolution while reducing the number of delay elements required, and seamlessly integrates with a counter-based controller, extending the dynamic range to effectively cover a significantly larger sensing window. The CSA biochip, fabricated in 180-nm CMOS technology, achieves results with an overall sensitivity of 880 code/fF. This achievement translates into an sensing resolution of 1.13 aF, demonstrating its potential to further advance the development of CMOS-based cell-monitoring platform.**

***Index Terms*—digital-to-time converter (DTC), 2-D Vernier, capacitive sensor array (CSA), ts-TDC, lab-on-a-chip (LOC).**

I. Introduction

Capacitive sensor array (CSA) has gained prominence in the realm of life science applications, offering a range of advantages, such as label-free operation, lower noise, and scalability [1]. These platforms have found effective use in real-time cell viability detection and impedance measurements. With the rapid advancement of complementary metal-oxide-semiconductor (CMOS) technology, CMOS-based CSA enables the automation of bio-protocols, facilitating mass production and cost reduction [2]. Consequently, the Cell-on-CMOS platform has gained significant research interest among researchers.

Since the typical dimension of a single cell is approximately 10 µm × 10 µm, substantial circuit architectures for miniaturizing electrode cell (EC) have been developed [3], [4]. Nevertheless, limitations still persist, especially when it comes to the precise detection of individual cells rather than cell clusters. In response to the demand for single-cell detection capabilities, a time-sharing time-to-digital converter (ts-TDC) approach has been proposed [5]. Each EC occupied a minimal area of only 2.25 µm × 2.25 µm, and it incorporates fusion pixels designed for programmable cell-monitoring. However, the sensitivity issue due to the miniaturized electrode size remains a significant concern, particularly affecting the sensing resolution for analyzing cell morphology.

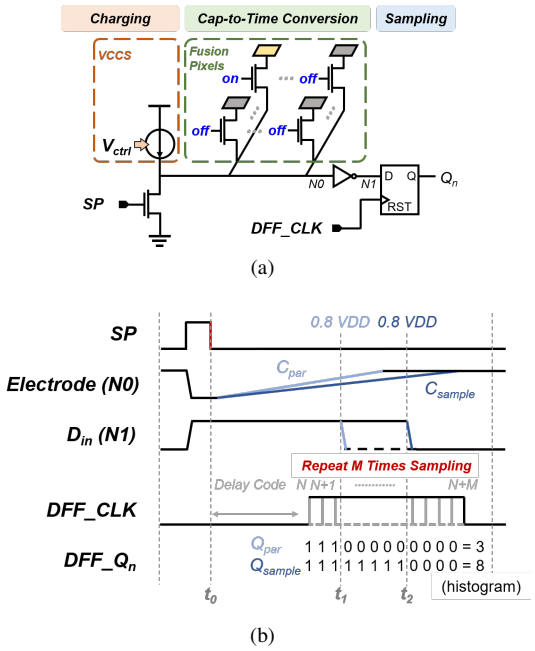


Fig. 1. Electrode cell. (a) Schematic of the EC. (b) Timing diagram of EC operation.

To address the challenge, this work focuses on enhancing the overall sensitivity by extending the sensing window within the capacitance-to-time conversion. This is achieved by employing a voltage controlled current source (VCCS) in the charging unit, as illustrated in Fig. 1(a). This expansion of the sensing window necessitates the subsequent sampling operation to cover a wider dynamic range effectively. Moreover, improving the timing resolution and enhancing noise tolerance enables more precise quantization.

In this paper, we introduce a novel 2-D vernier digital-to-time converter (2D V-DTC) designed to enhance the sampling operation of the ts-TDC approach. The integration of the 2-D vernier structure and a counter-based controller aims to achieve 2.56-µs dynamic range and 31.25-ps resolution,

exhibiting fourfold improvement on both metrics compared to the delay pulse delay generator (DPDG) in previous work [5]. Additionally, by combining it with delay-locked loop (DLL) based circuit design, the implementation enables calibration for process-voltage-temperature (PVT) variations. This collaborative effort significantly enhances the quality of bio-detection in the cell-monitoring platform.

The remainder of this paper is organized as follows. Section II introduced the design concepts of the proposed 2D V-DTC, while the circuit implementation is presented in Section III. The measurement results are reported in Section IV, and conclusions are drawn in Section V.

II. 2-D Vernier Digital-to-Time Converter

A. Sampling Operation for EC

The sampling operation for EC is illustrated in Fig. 1(b). Initially, the sensing pulse (*SP*) is set low to charge the EC, providing a sensing window at N0 for subsequent quantization. When the EC reaches 0.8VDD, the output of following hi-skewed inverter (N1) is switched to logic low. The D-flip flop (DFF) is then sampled at a specific timing delay programmably determined by delay code.

The operation waveform depicted in Fig. 1(b) shows two conditions: without sample (C_{par}) and with sample (C_{sample}). These conditions present sensing windows with varying lengths due to the change in capacitance. The sensing process is repeated with various amounts of timing delay across the sensing window. By summing all output results of the DFF, we can obtain the precise timing difference between both logic transition locations, thus generating the corresponding sensing result. In summary, the ts-DTC based approach enables the sampling of the entire CSA using a single DTC.

B. Delay Generation

The timing diagram shown in Fig. 2(a) illustrates the process of delay generation. In contrast to the conventional RC-delay based method [6], which introduces a controlled delay to the transition edges of its input signal, our proposed design initiates circuit operation upon receiving the trigger signal (*SEN_TRI*). This results in the generation of both leading and lagging output signals (*V_START, V_STOP*), directly utilized for EC's charging (*SP*) and sampling (*DFF_CLK*). The delay generation is detailed in the equation of $D_{total} = D_3 + (D_2 - D_1)$. The total delay amount (D_{total}) precisely corresponds to the timing difference between the negative edge of *V_START* and the positive edge of *V_STOP*, programmably determined by the external delay code. To achieve the desired high resolution, we employ a 2-D vernier structure, inspired by [3], as a fine-tuning stage to control the first two factors (D_1, D_2). The integration with a counter-based controller, serving as coarse-tuning stage, determines the third factor (D_3) to meet the requirement of a wide dynamic range.

C. 2-D Vernier Structure

In coarse-tuning stage, a counter-based controller is designed to achieve a resolution of $T_{coarse} = 2.5ns$. In the fine-tuning stage, the 2-D vernier structure is implemented using

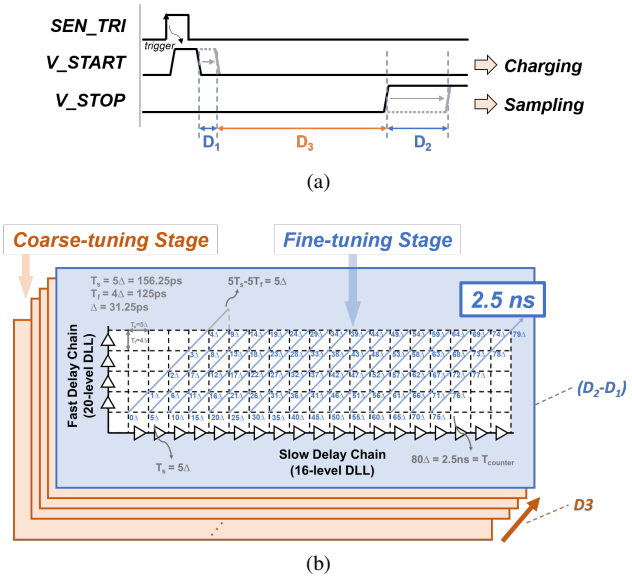


Fig. 2. Proposed 2D V-DTC. (a) Timing diagram. (b) Conceptual diagram.

two types of delay units, slow and fast (T_s, T_f), respectively. The resolution of 2D V-DTC is defined as the timing difference between these delay units, i.e., $T_{res} = T_s - T_f$. Compared to other types of vernier structure, the 2-D vernier structure uses reduced number of delay units to cover same dynamic range.

As depicted in Fig. 2(b), the 2-D vernier structure divides a conventional long vernier delay line into multiple sections, creating 16 generation lines with 16 transition locations, each separated by 5th-generation points. Upon closer inspection, the delay at the extended sixth-generation point of the first-generation line is equal to $6T_s - 6T_f = 6T_{res}$, while the first-generation point of the second-generation line is equal to $2T_s - T_f$. To ensure a smooth transition between each generation line, both conditions should yield identical timing delays. This linearity issue implies that the slow and fast delay units should be regulated to have the relationship $4T_s = 5T_f$. Therefore, we design both delay units as $T_s = 5\Delta = 156.25ps$ and $T_f = 4\Delta = 125ps$. This results in a resolution of $T_{res} = \Delta = 156.25ps - 125ps = 31.25ps$ in our work. Additionally, to align with the resolution of the coarse-tuning stage, the total generation points in the fine-tuning stage are expanded to 80. Furthermore, we implement DLL-based circuit design to precisely control and stabilize the delay amounts of both delay units, effectively mitigating the impact of PVT variations and preserving the stability and linearity of delay generation.

III. Circuit Implementation

A. DTC System

The circuit design of the 2D V-DTC is illustrated in Fig. 3, comprising five key components: (1) clock-multiplying circuit, (2) vernier DLLs for the fine-tuning stage, (3) counter-based controller for the coarse-tuning stage, (4) serial-to-parallel (S2P) converter, and (5) pulse generator (PG).

The clock-multiplying circuit and vernier DLLs, which include 16-level and 20-level DLLs, initially conducts frequency

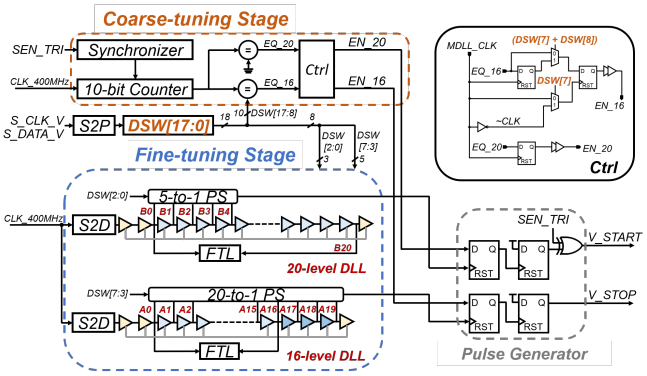


Fig. 3. Circuit diagram of the proposed 2D V-DTC.

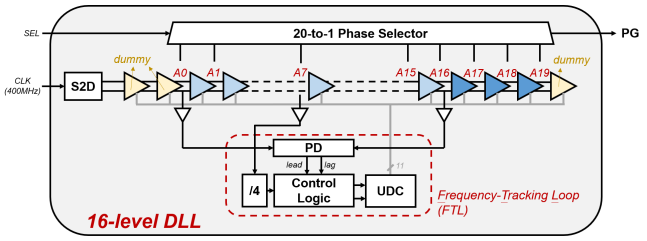


Fig. 4. Vernier delay-locked loops.

tracking to generate a 400 MHz clock signal. An 18-bit delay code (*DSW[17:0]*) is externally set to achieve the desired delay using the S2P converter. The first 10 bits are directed to the counter-based controller for coarse-tuning, while the last 8 bits are sent to the vernier DLLs for fine-tuning. The counter-based controller is activated by the *SEN_TRI* and provides two enabling signals (*EN_16, EN_20*) to the PG. Finally, the PG uses the selected clock phases from the vernier DLLs to generate *V_START* and *V_STOP*.

B. Vernier Delay-Locked Loops

The vernier DLLs consist of 16-level and 20-level DLLs. As illustrated in Fig. 4, the 16-level DLL comprises a digitally controlled delay line (DCDL), a frequency-tracking loop (FTL), and a 20-to-1 phase selector (PS), functioning as the slow delay chain. The 16 delay elements (light blue units) in the middle of the DCDL are synchronized to 400 MHz using the FTL. The subsequent 3 delay elements (navy blue units) are used to extend phases to 20. In a structure similar to the 16-level DLL, the 20-level DLL along with 5-to-1 PS is designed as the fast delay chain. The middle 5 bits of the delay code are for the phase selection of 16-level DLL, while the last 3 bits are designated for the 20-level DLL. The selected phases are specified to trigger the subsequent operations in the PG.

C. Counter-based Controller

As illustrated in Fig. 3, the counter-based controller primarily consists of a synchronizer, 10-bit counter, equal logic, and control logic. The operational waveform is depicted in Fig. 5. The synchronizer first receives the *SEN_TRI*, and then initiates the calculation of the 10-bit counter. When the value

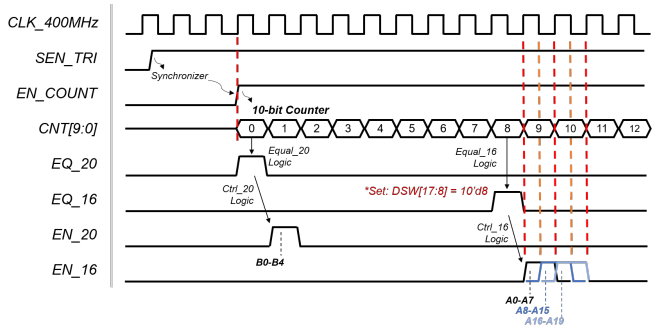
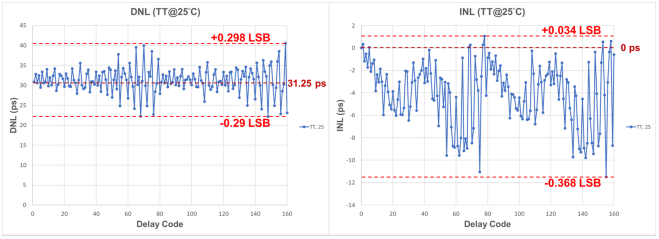


Fig. 5. Operation waveform of counter-based controller.



(a) (b)

Fig. 6. Post-simulation results (TT@25°C). (a) DNL. (b) INL.

TABLE I
POST-SIMULATION RESULTS OF THE PROPOSED 2D V-DTC.

Corner	FF, 0°C	TT, 25°C	SS, 50°C
DNL (LSB)	+0.132 / -0.131	+0.298 / -0.29	+0.29 / -0.236
INL (LSB)	+0.051 / -0.17	+0.034 / -0.368	+0.248 / -0.317

of the activated counter remains the same and to zero, the first equal logic (*EQ_20*) switches to logic high, generating the corresponding control signal (*EN_20*). Similarly, when the value of the active counter matches the target value (*DSW[17:8]*), the second equal logic (*EQ_16*) switches to logic high, producing another control signal (*EN_16*). Both control signals are transmitted to the PG.

D. Post-Simulation Results

To verify the functionality, the post-simulation results is presented in Fig. 6 for the first 160 delay codes, encompassing two complete fine-tuning stages and the junction between them. Under TT@25°C corner, the worst-case differential nonlinearity (DNL) and integral nonlinearity (INL) are +0.298 and -0.368 LSB, respectively. Furthermore, the performance under FF@0°C and SS@50°C corners are evaluated to account for bio-experiments, and the results are shown in Table I.

IV. MEASUREMENT RESULTS

The ts-TDC based CSA biochip is fabricated in 180-nm technology. As depicted in Fig. 7, the CSA is comprises of 480 × 960 fusion pixels, and the chip occupies an area of 2.576 mm × 3.728 mm. The proposed 2D V-DTC is positioned at the lower right corner of the CSA, occupying an area of 1.049 mm × 0.361 mm.

TABLE II
PERFORMANCE COMPARISON OF CMOS-BASED CSA.

	This Work	VLSI'17 [7]	TBCAS'15 [8]	TBCAS'18 [9]	TBCAS'22 [3]	TCASII'23 [5]
Technology	**180 nm**	130 nm	250 nm	350 nm	350 nm	180 nm
Application	**Cell Monitoring**	Cell volume growth monitoring	Detection of bacterial cell	Measurement of cell proliferation	Droplet analysis	Real-time monitoring
Array #	**480 × 960**	3 × 4	16 × 16	4 × 4	16 × 16	480 × 960
Pixel Size (μm^2)	**2.25 × 2.25**	90	14 × 16	30	35 × 30	2.25 × 2.25
Architecture	**ts-TDC**	CFC	CVC	CFC	CBCM	ts-TDC
Method	**Digital**	Digital	Analog	Digital	Digital	Digital
Resolution	**1.13 aF**	10 aF	450 aF	14.4 aF	150 aF	145 aF
Sensitivity	**880 code/fF**	235 mV/fF	55 mV/fF	590 kHz/fF	N/A	6.896 code/fF
Input Dynamic Range	**40 fF**	± 100 fF	0.45fF-57fF	12 fF	100 fF	N/A

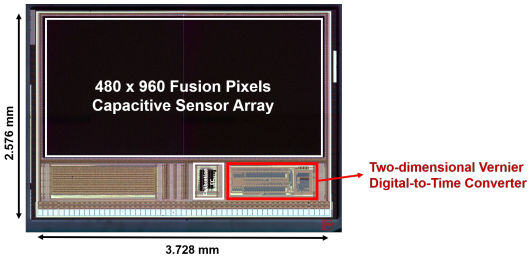


Fig. 7. Die photo.

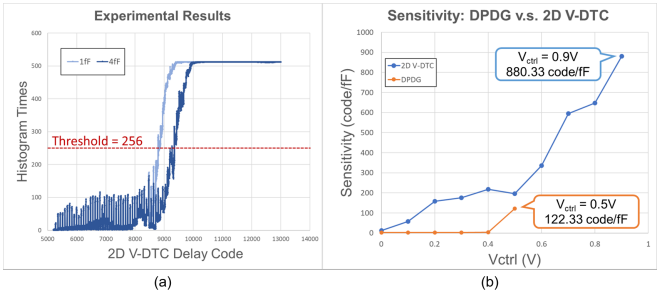


Fig. 8. Fixed Capacitance Testing. (a) Experimental results. (b) Comparison.

A. *Fixed Capacitance Testing*

The fixed capacitance testing is performed to evaluate the sensitivity performance. We utilized calibration ECs connected to specific fixed MIM capacitors of 1fF and 4fF involving a range of real biological samples. A 512-fold multiple sampling approach and data classification are employed to conduct noise-canceling. Results exceeding a threshold of 256 are classified as 1, while those below the threshold are marked as 0.

Fig. 8(a) illustrates the variation in capacitive response across multiple delay codes under room temperature of 27°C. The light blue curve corresponds to a 1fF capacitance, exceeding the threshold at delay code 8784, while the navy blue curve represents a 4fF capacitance, with its delay code surpassing the threshold at 9344. This outcome indicates that with a capacitance difference of 3fF, there is an corresponding 560-unit variation in the delay code.

B. *Sensitivity Analysis*

This testing enables a comparison of the sampling block between the proposed 2D V-DTC and the DPDG [5], as depicted in Fig. 8(b). In the case of our proposed 2D V-DTC, the dynamic range effectively covers the entire sensing window under the VCCS is set to 0.9V. The blue curve represents the overall sensitivity, capable of detecting approximately 1fF, corresponding to 880 delay code changes. Conversely, in the case of the previous DPDG, maximum sensitivity is achieved when the VCCS is set to around 0.5V, as indicated by the orange curve. Under this condition, 1fF corresponds to 122 delay code changes. These results reveals that our proposed work achieves a outstanding 7.196x increase in sensitivity compared to the previous implementation.

C. *Performance Comparison*

The performance comparison of prior CMOS-based CSA designs is presented in Table II. In CSA design, both pixel size and overall sensitivity are critical factors that directly influence the quality of bio-detection. The 2D V-DTC, proposed in this work, provides the ts-TDC approach with a sensitivity of up to 880 code/fF, equivalent to a sensing resolution of 1.13 aF. Compared to related works, our biochip demonstrates competitive performance in the Cell-on-CMOS platform.

V. CONCLUSION

This paper presents a novel 2D V-DTC with 31.25-ps resolution and 2.56-µs dynamic range to improve the overall sensitivity of the CSA system. The 2-D vernier structure is designed for fine-tuning to achieve sufficient resolution without requiring a large number of delay units. The integration of a counter-based controller for coarse-tuning extends the dynamic range to cover a significantly larger sensing window. Fabricated in 180-nm CMOS technology, the ts-TDC based CSA biochip is measured through the sensitivity analysis. As a result, this work achieves an outstanding sensing resolution of 1.13 aF, advancing the state-of-the-art CMOS-based CSA design. Through the incorporation of low-power technique and high conversion rate in the future work, this design can further promote the development of the cell-monitoring platform.

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