A Programmable CMOS Dielectrophoresis Array Chip with 128×128 Electrodes for Cell Manipulation

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***Abstract*—Dielectrophoresis (DEP) is a powerful technique for manipulating biological cells. Yet, its widespread application has been limited by traditional glass-based chips with static electrode configurations that often require integrated microfluidic systems. This paper presents a novel DEP array chip fabricated in a standard CMOS process, featuring a 128×128 electrode matrix capable of generating dynamic, programmable electric field patterns that can be tailored to meet specific requirements for different use cases. Experiments have demonstrated the ability of the chip to manipulate fibroblast and THP-1 cells, with fibroblast movement observed at a velocity of 10µm/s with a DEP frequency of 800kHz and a peak-to-peak DEP voltage of 1.8V. The chip is designed for compatibility with standard petri dishes, obviating the requirement for microfluidics and facilitating its integration with traditional cell culture protocols. Our results indicate the chip's potential as a versatile tool for cell biology research and applications.**

***Index Terms*—Dielectrophoresis, DEP, CMOS, programmable, lab-on-a-chip, cell manipulation**

I. Introduction

The field of microscale particle manipulation has seen significant advancements over the past few years. This progress is driven by the increasing demand for high-throughput and high-precision techniques in various applications, including cell sorting [1], drug delivery [2], and biological studies. Recently, CMOS capacitive sensing chips have become increasingly popular in cell quality detection due to their high sensitivity and resolution [3]–[7]. However, once desired and undesired cells have been identified, a label-free method is required for their separation [3], [8]. Fig. 1 illustrates the relocation of inferior cells to the corner to make room for high-quality cells.

Dielectrophoresis (DEP), a technique that employs non-uniform electric fields to exert forces on particles, shows potential in addressing this requirement [9]. It facilitates the manipulation and separation of cells without the need for labeling. However, the practical application of DEP is often hindered by the lack of suitable platforms capable of generating complex and programmable electric field patterns [10]–[12].

CMOS technology emerges as a promising solution to this problem. Its integrated control circuitry enables the generation of programmable electric field patterns [13], [14]. Moreover, the mass-production nature of CMOS technology provides the foundation for its widespread use.

This paper presents a programmable CMOS DEP array chip with 128×128 reconfigurable electrodes for cell manipulation. The chip utilizes lateral negative DEP (nDEP) forces to repel cells from the chip surface, reducing the risk of cell adhesion and eliminating the need for a top plate. The petri dish compatibility of the chip allows for easy integration into existing cell culture processes, eliminating the need to modify the current bio-protocol.

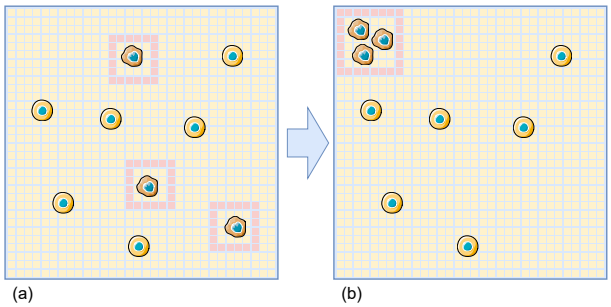

Fig. 1. Move inferior cells to the corner. (a) Once inferior cells are identified, electrodes around them are activated to trap the cells. (b) Progressively change the activated electrode to move the trapped cells to the corner.

The structure of this paper is as follows: Section II explains the principle of DEP and how the chip utilizes it. Section III delves into the specifics of the chip's implementation, including its architecture and packaging. Section IV presents the experimental results, and Section V concludes the paper.

II. Principle of DEP

DEP is a phenomenon in which a force is exerted on a dielectric particle when exposed to a non-uniform electric field [15]. This force is not dependent on the particle's charge, but on its polarizability, which is the ability of the particle to form instantaneous dipoles in response to an external electric field [16]. The direction of the DEP force depends on the relative polarizability of the particle and the surrounding medium. The DEP force (F_{DEP}) can be expressed by the following equation [17]:

$$F_{DEP} = 2\pi r^3 \varepsilon_0 \varepsilon_m Re[f_{CM}] \bigtriangledown E_{rms}^2 \tag{1}$$

where r is the radius of the particle, ε_0 is the permittivity of the vacuum, ε_m is the dielectric constant of the medium, f_{CM} is a complex variable known as Clausius-Mossotti factor, E_{rms} is the root-mean-square value of the applied electric field.

The Clausius-Mossotti factor is

$$f_{CM} = \frac{\varepsilon_p^* - \varepsilon_m^*}{\varepsilon_p^* + 2\varepsilon_m^*} \tag{2}$$

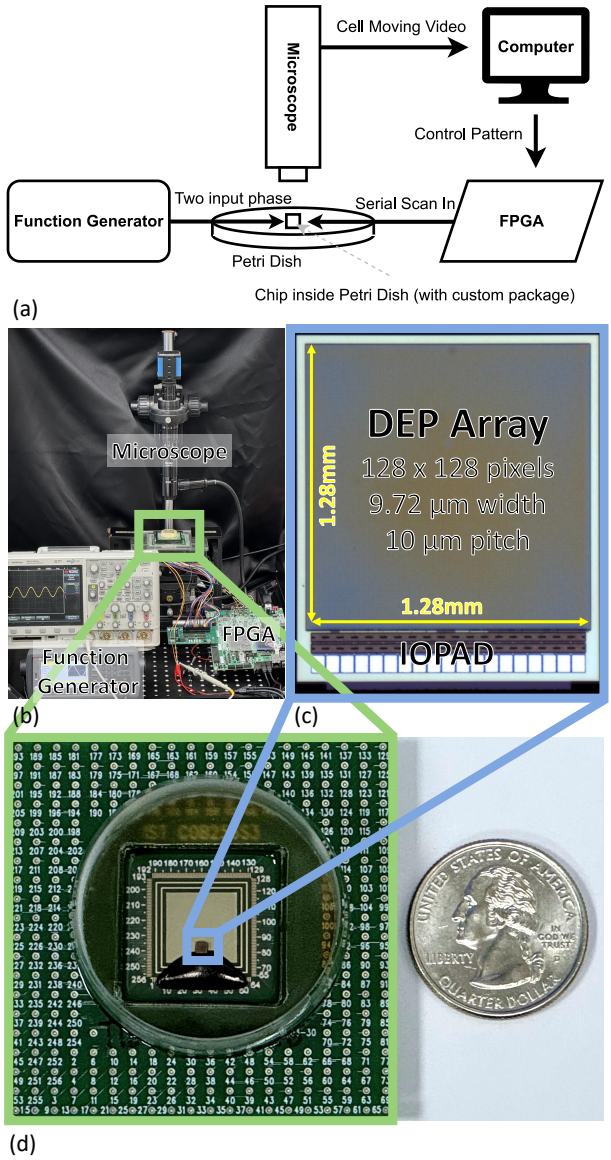

Fig. 2. (a) Schematic of the CMOS DEP array system. (b) Picture of the system. (c) Die photo. The quarter is included for scale. (d) Petri dish compatible DEP chip. The laser-cut petri dish was glued to the PCB using EPOXY.

where ε_p^* and ε_m^* are the complex permittivity of the particles and the medium, respectively, and are given by $\varepsilon^* = \varepsilon - j\sigma/\omega$, where σ is the conductivity and ω is the frequency.

When the real part of f_{CM} is positive, the particle is more polarizable than the medium and experiences positive DEP, moving towards regions of high electric field (usually close to electrodes). On the contrary, when the real part of f_{CM} is negative, the particle experiences a negative DEP and moves toward regions with low electric field. Because a positive DEP may cause the particle to stick to the surface of the chip, our chip utilizes a negative DEP to manipulate the particles.

The voltage of the top metal electrodes on the chip can be selectively programmed to mirror one of the two analog inputs on the chip. When an adjacent electrode selects a different

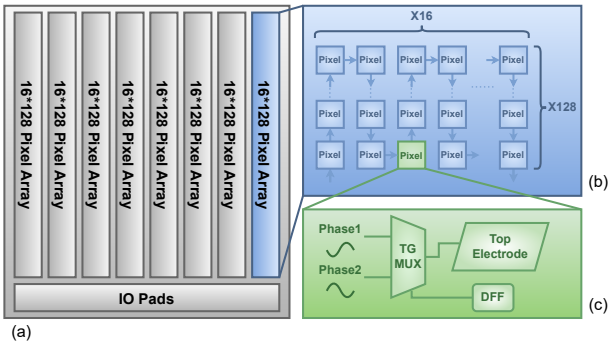

Fig. 3. Chip architecture. (a) The chip is composed of eight scan chains, each of which consists of 16×128 pixels connected together. (b) Each pixel in the scan chain is connected to the subsequent pixel, enabling the input pattern to be scanned in a sequential manner. (c) Each pixel is composed of a TGMUX and a DFF. The content of the DFF controls whether the signal input to the top electrode is in Phase 1 or Phase 2.

input voltage, a potential difference is created between the electrodes. This leads to a programmable non-uniformity in the electric field above the chip, which in turn exerts a DEP force on the particles.

III. Implementation

A. System Overview

Fig. 2(a) outlines the five primary components of the system, including a computer, a field-programmable gate array (FPGA) embedded within the Xilinx ZCU106 board, a DEP chip, a function generator, and a microscope.

The computer, equipped with custom-made Python software, is responsible for generating the required pattern for cell manipulation. The pattern is then transmitted to the FPGA via the UART protocol. The FPGA then disassembles the pattern into eight sequential snake scan data streams, which are distributed to the corresponding scan chains of the chip. The function generator feeds the chip with two input voltage functions, the specifications of which depend on the type of particles being manipulated. A long working distance microscope, positioned above the chip, monitors the movement of the cells. The video is then sent back to the computer for the generation of the next pattern.

Since the DEP chip does not require high voltage for cell manipulation, it can directly utilize the 1.8V power supplied by the FPGA. This simplifies the design of the power supply, resulting in a more compact and user-friendly system.

B. Chip Architecture

The architecture of the DEP chip is shown in Fig. 3. The chip is composed of a 128×128 pixel array, in which each pixel contains a D flip-flop (DFF) and a transmission gate-based analog multiplexer (TGMUX), as shown in Fig. 3(c). The DFF stores the input pattern, while the TGMUX selects the top electrode voltage to follow either Phase 1 or Phase 2 based on the content of the DFF. Both phases are global analog signals that are inputted to the chip from an external function generator. By arranging these pixels and connecting the output

TABLE I
CHIP INFORMATION

Process	TSMC 0.18μm 1P6M CMOS
Core Voltage	1.8V
Number of Pixels	128×128
Pixel Size (μm^2)	10×10
Chip Size (mm^2)	1.47×1.28
Electric Field	Programmable Lateral
DEP Voltage	1.8V
DEP Frequency	DC-1MHz

of one DFF to the input of the next in a snake scan fashion, a daisy chain structure is formed, as shown in Fig. 3(b). To avoid the high latency caused by the scan chain structure, the entire chip is divided into eight independent scan chains, as shown in Fig. 3(a). This also reduces the possibility of data transfer errors caused by global clock instability.

One advantage of directly inputting analog signals using a function generator is the flexibility of parameter adjustment. This gives us the ability to adapt to different experimental requirements quickly and accurately. However, the test results show that if the input frequency exceeds 1MHz, the enormous load of the global signal can cause a voltage drop of more than 20%. Detailed information on the proposed chip is given in Table I.

When selecting the electrode, Metal 6 is the default top electrode layer in the standard 0.18μm 1P6M process. However, this choice poses challenges for DEP applications, as depicted in Fig. 4. The top metal layer, designed for power distribution, is considerably thicker than other layers, which inadvertently increases the electrode spacing by approximately a factor of five compared to a Metal 5 electrode. This increased spacing decreases the strength of the electric field, leading to a weaker DEP force. Additionally, the standard passivation layer required above Metal 6 is approximately four times thicker than the dielectric layer between Metal 5 and Metal 6, further enlarging the gap between the cells and the electrodes and thus attenuating the DEP force. The lack of planarization of the passivation layer also introduces surface roughness that can impede cell movement. In contrast, the dielectric layer between Metal 5 and Metal 6 is planarized, offering a smoother surface that is beneficial for cell manipulation. Therefore, Metal 5 is a superior electrode choice for DEP applications.

C. Packaging

The biocompatible packaging of the DEP chip enables safe and effective interaction with biological systems. This package is designed to prevent any possible damage to the chip's electrical components and ensure optimal performance in a biological environment. The packaging process involves several steps. First, an insulating glass is placed underneath the chip to prevent the solution from contacting the PCB ground. The chip's pads are strategically positioned on one side to optimize the surface area for the experiment. To insulate the bonding wire from the solution in the petri dish, a black epoxy (JA126-29) is used. Finally, a medical epoxy (302-3M, EPOTEK) is used to adhere the petri dish to the PCB. The attached PCB replaces the bottom of the petri dish, providing direct contact between cells and the chip. The final product is shown in Fig. 2(d). This petri dish-compatible DEP chip can be directly placed into an incubator for cell culture. When the cells need to be moved, the entire chip can be transferred to our system for cell relocation.

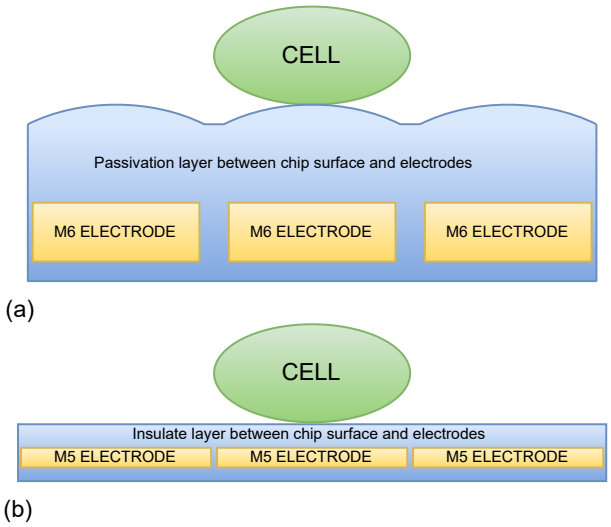

Fig. 4. Illustration of the distance between the cell and electrodes, the surface roughness, and the gap between electrodes. (a) The use of standard Metal 6 and a standard passivation layer results in significant surface roughness, making the movement of cells on the chip surface more difficult. (b) The use of Metal 5 as the top electrode and a thin dielectric layer reduces the electrode-cell distance by 4 times and the gap between electrodes by 5 times, resulting in a stronger electric field and greater DEP force.

IV. EXPERIMENTAL RESULTS

A. THP-1 Cell Patterning by Programmable Electric Fields

This experiment demonstrates the effectiveness of the programmable electric field in patterning human monocytic leukemia cells (THP-1). The pattern in Fig. 5(a) was loaded onto the chip before the cells were added. The two DEP phases are 400kHz sinusoidal waves with a 180-degree phase shift. Three minutes after adding the cells, the phrase "ISCAS 2024" is clearly visible in Fig. 5(b).

B. Multi-Attempt Cell Partitioning

The second experiment partitioned fibroblast cells into two groups using a sequence of patterns. A sequence of patterns is a series of predesigned electric field patterns sent to the chip with a time delay to move the cell incrementally. In this case, the pattern is designed with an outer ring to keep the cell on the chip and two lines that gradually move away from the center of the chip, one pixel at a time, as shown in Fig. 6(a).

Due to the varying electrical characteristics of each cell, a single partitioning attempt may not be sufficient. By taking advantage of the programmability of the chip, we can perform multiple partition attempts in a single experiment. Fig. 6(c) shows the result of partitioning fibroblast cells after 3 pattern

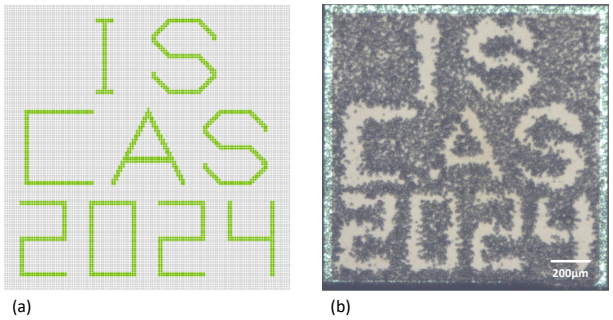

Fig. 5. The THP-1 cells are moved by the DEP force with a programmed pattern. (a) Two phases are configured in the electrode array to display the 'ISCAS 2024' pattern, with two colors indicating the two different phase voltages applied to the top electrode. (b) THP-1 cells arranged into the 'ISCAS 2024' pattern, viewed under an optical microscope.

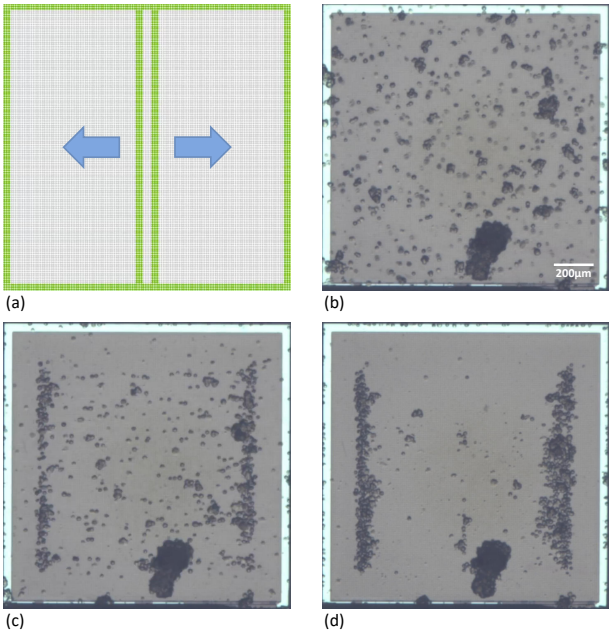

Fig. 6. Partitioning fibroblast cells into two groups using a DEP chip. (a) An example input pattern used in the sequence, with subsequent patterns diverging the middle two lines as indicated by the arrow. Patterns are switched at 1-second intervals. (b) Before the application of the DEP sequence. (c) After three cycles of the DEP sequence. (d) After fifteen cycles of the DEP sequence. The entire process took 15 minutes.

sequences. Approximately 50% of the cells are partitioned. With 15 pattern sequences, over 90% of the cells are partitioned, as shown in Fig. 6(d).

C. Individual Particle Positioning

One application of single cell positioning is to concentrate suboptimal cells during culture to free up space for higher-quality cells. The third experiment was designed to illustrate this concept. Initially, 10μm and 20μm particles are mixed as depicted in Fig. 7. A sequence of patterns is then applied to selectively move the 20μm particles to the upper left corner while keeping the 10μm particles stationary.

In conclusion, the experimental results confirmed the ability of the CMOS DEP chip to generate complex, programmable

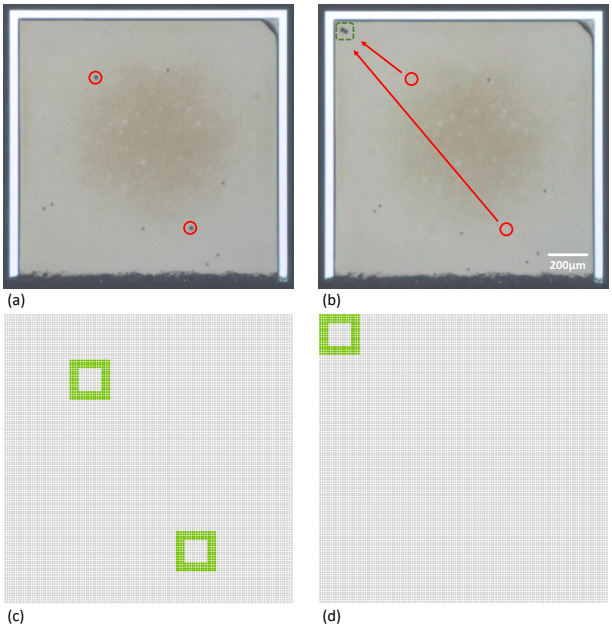

Fig. 7. (a) Initial distribution of 20μm and 10μm polystyrene particles. (b) Distribution after moving 20μm particles to the upper left corner. (c) Electric field pattern at the start of the sequence. (d) Electric field pattern at the end of the sequence. The entire process took 80 seconds.

electric field patterns for individual particle and cell positioning. Future efforts will focus on refining the DEP pattern and sequence to enhance sorting accuracy and speed and expanding the range of particle types that can be effectively manipulated.

V. Conclusions

In conclusion, a programmable CMOS DEP array chip with 128×128 electrodes is presented. Its programmability enables precise control of the surface electric field, making individual cell manipulation possible. The biocompatibility package ensures seamless integration with existing lab configurations.

Looking ahead, our goal is to incorporate a capacitive sensing component into the chip, enabling the detection and tracking of cells without the need for a microscope. This will simplify the system, enhance user-friendliness, and make it more compact, portable, and cost-effective. This progression will also lay the groundwork for the chip's integration into more feature-rich lab-on-a-chip systems, potentially unlocking new opportunities for automated biological experiments.

In summary, the petri dish compatible, programmable DEP chip represents a transformative innovation in cell manipulation, providing a versatile, adaptable, and highly precise tool for researchers. With planned enhancements, we foresee our chip continuing to redefine the limits of what is achievable in this field.

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