# A Programmable CMOS DEP Chip for Cell Manipulation

Wen-Yue Lin, Lin-Hung Lai, Yi-Wei Lin, Chen-Yi Lee

Abstract—This work presents a programmable CMOS DEP chip that allows real-time control over the spatial distribution of DEP force, enabling controlled cell movement on the chip surface, from single-cell manipulation to multi-cell patterning. Implemented on a standard 0.18 µm CMOS process without post-processing, the chip features a 128 × 128 array of individually controllable 10 µm microelectrodes with 0.28 µm spacing. Utilizing Metal 5 electrodes in a 1P6M process, the chip achieves particle manipulation speeds up to 27 µm/s while operating at only 1.8 V, preserving cell viability as confirmed through post-DEP assessments. The implementation of time-sharing patterns enhances manipulation precision by creating distinct boundaries between phases. Experiments demonstrate the chip's capabilities in particle patterning, concentration control, and singleparticle manipulation, all performed sequentially on the same chip. Additionally, stem cell aggregation control demonstration offers possibilities for future differentiation studies. With its reconfigurability, this DEP chip offers promising solutions to technical challenges in cell preparation, drug screening, and other biological applications.

*Index Terms*—Cell manipulation, dielectrophoresis, dynamic reconfiguration, cell patterning, particle concentration control, cell aggregation, single cell manipulation, lab-on-a-chip.

## I. INTRODUCTION

C ELL manipulation is a fundamental technique in biological research and applications, allowing for control and analysis of cell arrangements and behaviors [1]. In tissue engineering, two-dimensional cell manipulation helps form structured cell patterns for studying cell interactions [2]. In stem cell research, these techniques are vital for modulating cell aggregation, which in turn affects cell fate decisions and differentiation [3]–[5].

Various cell manipulation methods have been developed [6], including optical tweezers [7], [8], acoustic tweezers [9], magnetic manipulation [10], and dielectrophoresis (DEP) [11]. Each method has unique advantages and limitations. Among them, DEP stands out for its label-free nature, ability to handle large numbers of cells simultaneously, and outstanding biocompatibility by leveraging interactions between non-uniform electric fields and the dielectric properties of cells [12].

However, traditional DEP devices suffer from several limitations, including high operating voltages and fixed electrode patterns. High operating voltages can compromise cell viability and induce undesired electrochemical reactions, while

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To address these challenges, there has been growing interest in developing DEP devices using complementary metal-oxidesemiconductor (CMOS) technology. The work by Manaresi et al. [14] demonstrated a CMOS chip with a 320 × 320 array of 20 µm microelectrodes for manipulating cells. This approach utilizes vertical DEP cages formed between the top plate and bottom electrodes to localize cells. While effective for controlling cell movement, it constrains the flexibility of manipulation strategies. More recently, Hunt et al. [15] presented an integrated circuit/microfluidic chip with a 128 × 256 array of 11 µm microelectrodes, capable of manipulating cells and droplets at speeds up to 30 µm/s. However, the square wave output on the electrode and the use of positive dielectrophoresis (pDEP) to attract cells towards the electrode could lead to cell adhesion on the chip surface, impeding further cell rearrangement.

This paper presents the design and implementation of a programmable DEP chip, fabricated using a standard 0.18  $\mu$ m CMOS process. The chip features a 128 × 128 array of individually controllable 10  $\mu$ m microelectrodes, enabling the dynamic reconfiguration of electric field patterns. The use of a standard CMOS process provides scalability and the potential for mass production. The chip operates at a low voltage of 1.8 V, which minimizes the risk of cell damage and undesired electrochemical effects. The electrode design enables particle manipulation at a speed of 27  $\mu$ m/s. By employing negative dielectrophoresis (nDEP) to repel cells away from the electrode, the chip reduces the risk of cell adhesion during manipulation.

The reconfigurable nature of the chip allows multiple experiments on the same sample and chip, reducing manual intervention and contamination risks associated with traditional singlefunction DEP chips. Precise control over cell positioning and patterning is important in fields such as tissue engineering and drug discovery [16]. For instance, cell patterning can be utilized to create complex tissue models that mimic in vivo conditions, enhancing the accuracy of pharmaceutical testing [17].

In our experiments, the chip demonstrated particle patterning, concentration control, and single-particle manipulation, all conducted sequentially on the same sample and chip. Using programmable patterns, the chip enabled induced pluripotent stem cells (iPSC) aggregates of various sizes on the same chip, supporting differentiation research. Cell viability assessments



Fig. 1. Principle of nDEP. Particle subjected to a force towards the region of lower electric field intensity.



Fig. 2. Non-uniform electric field generated by electrodes with different phase signals, resulting in a separation ridge that exerts a force on the particle.

indicated that the low-voltage operation and gentle manipulation conditions did not affect cell viability during the duration of the experiments.

The remainder of this paper is organized as follows. Section II presents the principle of DEP and how our chip utilizes it. Section III details the design and implementation of the DEP system. Section IV describes the pattern design considerations. Section V presents the experimental results. Section VI concludes the paper and outlines future research directions.

#### II. DIELECTROPHORESIS FUNDAMENTALS AND UTILIZATION

### A. Principle of Dielectrophoresis

Dielectric particles subjected to an electric field experience polarization, leading to the induction of equal amounts of positive and negative charges. In a non-uniform electric field, regions with higher field strength exert greater forces on these induced charges, resulting in a net force on the particle, as depicted in Fig. 1. This phenomenon is known as DEP.

Both the particles and the surrounding medium can induce charges. The direction of the DEP force is determined by the relative magnitudes of the charges induced in the particle and the medium. Fig. 1 illustrates a scenario where the medium induces a greater amount of charge, pushing the particle toward regions of lower electric field strength. This specific case is referred to as nDEP.

The magnitude and direction of the DEP force depend on various factors, including the particle's size, shape, and dielectric properties, as well as the properties of the medium and the frequency and gradient of the electric field. The timeaveraged DEP force can be mathematically expressed as:



Fig. 3. Separation ridge generated by an array of electrodes. Particles experience greater force near the separation ridge.

$$F_{\text{DEP}} = 2\pi r^3 \varepsilon_m \text{Re}\{f_{CM}\} \nabla E_{\text{rms}}^2 \tag{1}$$

where r is the particle radius,  $\varepsilon_m$  is the permittivity of the medium, E is the electric field, and  $\text{Re}\{f_{CM}\}$  is the real part of the Clausius-Mossotti (CM) factor.

The CM factor  $f_{CM}$  is defined as:

$$f_{CM} = \frac{\varepsilon_p^* - \varepsilon_m^*}{\varepsilon_p^* + 2\varepsilon_m^*} \tag{2}$$

where  $\varepsilon_p^*$  and  $\varepsilon_m^*$  are the complex permittivities of the particle and the medium.

The sign of the real part of the CM factor,  $\operatorname{Re}\{f_{CM}\}$ , determines the direction of the DEP force. When  $\operatorname{Re}\{f_{CM}\} > 0$ , particles experience pDEP and are attracted toward regions of higher electric field intensity. Conversely, when  $\operatorname{Re}\{f_{CM}\} < 0$ , particles experience nDEP and are repelled from these regions.

Since the CM factor depends on the dielectric properties of both the particle and the medium, adjusting the properties of the suspending medium and the frequency can change the DEP response from nDEP to pDEP. In this paper, nDEP was used to prevent cells from adhering to the chip surface. However, by tuning the medium properties and frequency, pDEP can also be observed on our chip during experiments.

## B. DEP Utilization on CMOS Chip

The DEP chip comprises a  $128 \times 128$  electrode array, where each electrode is capable of independently selecting one of two analog signals from the chip's inputs for transmission to the surface. If adjacent electrodes select different signals, a nonuniform electric field is generated between the electrodes, as illustrated in Fig. 2 and Fig. 3. The force occurs at the gap between adjacent electrodes, pushing outward from the gap and forming a distinct boundary similar to a ridge. Therefore, we refer to this as a 'separation ridge.' The arrangement of separation ridges can be adjusted by programmably selecting the DEP signals on the electrode surface, thereby allowing for programmable control of particle positions.

Due to stronger electric fields in the gaps between electrodes, using pDEP to attract particles can cause adhesion of



Fig. 4. Design of the DEP chip. (a) Scan chain architecture with arrows indicating signal flow. (b) Global signal distribution for the two DEP phases. (c) Transistor-level schematic of the pixel circuit.

particles to the chip surface, obstructing subsequent manipulation. Therefore, our chip utilizes nDEP to control particle positions.

#### **III. DEP CHIP IMPLEMENTATION**

The chip implementation can be divided into circuit design, electrode design, and biocompatible packaging. The circuit design ensures programmability and functionality, while the electrode design optimizes DEP performance. For packaging, we developed two methods: one supports experiments with low sample volumes, and the other ensures compatibility with existing cell culture protocols.

### A. CMOS Circuit Design

The objective of the circuit design is to provide programmable control of the electric field on the chip surface. To achieve this, each pixel must be individually controllable, allowing for the generation of non-uniform electric fields between pixels. The schematic and layout of the pixel circuit is provided in Fig. 4 and Fig. 5.

1) Pixel Circuit Design: The pixel circuit design focuses on ensuring individual pixel controllability. This requires a storage element to retain state information and a select element to channel the appropriate DEP signal based on the stored data. For the storage element, two candidates are considered: static random-access memory (SRAM) and D-type flip-flops (DFFs). Although SRAM is more compact [14], [15], DFFs are preferred for their purely digital nature, which improves the array's scalability and facilitates future integration with other functions like capacitive sensing [18]. For the select element, a transmission gate-based multiplexer (TGMUX) is chosen. This component is optimal for transmitting the analog DEP signal with minimal distortion, effectively bridging the digital



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Fig. 5. (a) Layout of the pixel circuit. (b) M5 electrode on top of each pixel circuit.

control from the DFF with the analog DEP requirements. The functionality and integration of these components are detailed in a transistor-level schematic, shown in Fig. 4(c).

2) Scan Chain Design: A scan chain architecture is used to efficiently program the large array of pixels. The scan chain serially connects the DFFs of each pixel, as shown in Fig. 4(a), allowing data to shift through the chain one bit at a time with each clock cycle. This design offers scalability and significantly reduces the required input/output pins. The chain can be easily extended to larger arrays by adding more DFFs in series without substantial changes to the overall architecture. In the proposed design, eight scan chains are implemented, each responsible for a  $16 \times 128$  array segment. This partitioning strategy enhances the scan speed by enabling parallel data loading across the eight chains. With a 10 MHz clock, the theoretical maximum refresh rate of the entire array is about 5,000 frames per second (5 kfps), which indicates that the pattern on the chip can be altered continuously at this rate. However, during pattern scanning, all DFF values are continuously updated, causing the electric field on the chip surface to fluctuate rapidly. For effective particle manipulation on the chip surface, each pattern must remain stable for a sufficient duration to avoid constantly fluctuating electric fields. To effectively manipulate particles on this surface, we define two temporal parameters: 'effective time' and 'transition time.' Effective time refers to the proportion of each frame during which the DEP pattern remains stable, whereas transition time is the duration required to switch between patterns. To achieve an effective time of 99%, the effective frame rate is approximately 50 fps.

3) Global Signals: DEP actuation requires two counterphase sinusoidal signals to generate the non-uniform electric field. However, generating these signals within each pixel is impractical due to the substantial circuitry required, which would significantly increase pixel size and compromise array density. To address this challenge, a global DEP actuation signal scheme is employed. In the proposed design, the two counter-phase DEP signals are generated off-chip by a function generator and fed into the chip as global signals, ensuring all electrodes receive the same voltage as depicted in Fig.



Fig. 6. Cross-sectional view of the process used. (a) Normal usage with the top metal layer as electrodes. (b) Proposed method using the second-highest metal layer as electrodes.

4(b). The frequency of these signals can be easily adjusted by the function generator to accommodate different samples and experimental requirements. In addition to the DEP actuation signals, a clock signal is distributed to all pixels to synchronize the operation of the scan chains, ensuring data loading across the array, while a global reset signal is connected to all DFFs to allow for the simultaneous initialization of all pixels to a known state.

#### B. Electrode Design

The electrode design plays a crucial role in determining the strength and distribution of the electric field, which directly influences the DEP force experienced by the cells. Three key factors in optimizing the electrode design are the size of the electrodes, the gap between adjacent electrodes, and the distance between the electrodes and the cells.

1) Size of Electrode: The size of the electrode determines the minimum resolution at which cells can be separated. To effectively manipulate individual cells, the electrode dimensions should be comparable to the size of the targeted cells. In our design, we have chosen an electrode size of 10  $\mu$ m, which is well-suited for the manipulation of most common cell types.

2) Gap Between Electrodes: The gap between adjacent electrodes is a crucial parameter in determining the strength of the electric field and, consequently, the DEP force. According to the DEP equation (1), the DEP force  $F_{\text{DEP}}$  is directly proportional to the gradient of the square of the electric field. The electric field strength E is given by E = V/d, where V is the voltage applied between the electrodes and d is the distance between them. By reducing the gap d between electrodes, we can achieve a higher electric field strength for a given applied voltage. This, in turn, enhances the DEP force experienced by the cells.

3) Gap Between Electrodes and Cells: The distance between the electrodes and cells significantly impacts the effec-



Fig. 7. (a) CMOS DEP array chip die photo. (b) Photo of electrodes. (c) SEM image of the chip surface with corner included, revealing the homogeneous and smooth texture of the surface as illustrated in Fig. 6(b)

tiveness of the DEP force. Since the electric field weakens with distance, minimizing this gap is crucial. In CMOS chips, the electrodes are typically covered by a passivation layer to protect the underlying metal from direct contact with the biological samples. However, a thicker passivation layer increases the distance between the electrodes and the cells, reducing the strength of the electric field experienced by the cells.

In standard CMOS processes, the top metal is thick since it is meant for power transmission. As a result, the design rules differ from other metal layers, requiring larger gaps between adjacent metals. To overcome these limitations within standard CMOS processes, we have adopted the second-highest metal layer (M5) as the electrode while omitting the topmost metal layer (M6), as depicted in Fig. 6. Additionally, we use only the insulating layer above M5 instead of the standard passivation layer. This design choice reduces the electrode-to-surface distance from approximately 4 µm to about 1 µm, bringing the samples closer to the electrodes and significantly enhancing the DEP force. Furthermore, using M5 reduces the spacing between electrodes by more than five times compared to M6, substantially increasing the electric field between electrodes and further intensifying the DEP force. The die photo and the surface of the chip are shown in Fig. 7.

#### C. Biocompatible Package

Two packaging methods for the CMOS DEP chip are proposed. The first method is designed for applications with limited sample availability, such as single-cell manipulation or rapid testing. The second method ensures compatibility with existing cell culture protocols.

1) Low Sample Volume Packaging: In applications that need to minimize sample consumption, we have adopted a packaging solution that enables cell manipulation with a sample volume of less than 1  $\mu$ L. Wire bonding is performed on the chip's surface pads to enable communication between the chip and external devices. Because conductive biological samples need to be applied directly onto the chip, a waterproof epoxy This article has been accepted for publication in IEEE Transactions on Biomedical Circuits and Systems. This is the author's version which has not been fully edited and content may change prior to final publication. Citation information: DOI 10.1109/TBCAS.2024.3514874



Fig. 8. Chip packaging. (a) Chip wire-bonded on one side to reduce sample volume. (b) Photograph of the chip with a glass top plate. (c) Photograph of the chip with a Petri dish.

encapsulation is applied over the bonding wires to ensure proper insulation. The packaging process was performed by a specialized service provider, where automated wire bonding and manual epoxy encapsulation were used. However, this packaging process inevitably adds height to the chip. To mitigate the impact of this additional height on sample volume requirements, we strategically placed all the pads on one side of the chip during the design phase [18], [19]. This approach ensures that the height occupied by the packaging does not affect the height of the chip's active area, thereby minimizing the sample volume required, as depicted in Fig. 8(a) and (b).

2) Petri Dish Packaging: To enable seamless integration with established cell culture protocols, we have adopted a packaging solution that modifies standard cell culture dishes [20]. By creating an opening at the bottom of a culture dish and attaching it to the low sample volume packaging described in the above section, we create a programmable culture device with a capacity of approximately 3 mL, as shown in Fig. 8(c). The increased culture medium volume is beneficial for cell growth and maintenance. This modified culture device is compatible with existing incubators, facilitating post-manipulation cell culture and long-term observations.

In terms of durability, we tested both packaging techniques with high-pressure water cleaning following biological experiments. This cleaning process did not cause any damage to the chip or its packaging, ensuring the reliability of our proposal.

## D. System Overview and Testability

The CMOS DEP chip system comprises six primary components, as illustrated in Fig. 9(a). These include a computer, a field-programmable gate array (FPGA) embedded within the Xilinx ZCU106 board, a DEP chip, a function generator, an oscilloscope, and a microscope. The computer, equipped with bespoke Python software, generates the required pattern for particle manipulation and transmits it to the FPGA via the Uni-



Fig. 9. CMOS DEP array system. (a) Block diagram of the system. (b) Photograph of the actual system setup.

versal Asynchronous Receiver/Transmitter (UART) protocol. The FPGA disassembles the pattern into eight sequential data streams, which are distributed to the chip's corresponding scan chains. The function generator provides the chip with two DEP signals based on the type of particles being manipulated. A long working distance microscope, positioned above the chip, monitors the particles' movement and sends the video back to the computer for the next pattern generation. The DEP chip, operating at 1.8 V supplied directly by the FPGA, simplifies the power supply design, making the system more compact and user-friendly.

To ensure proper chip functioning, we implemented two testability features. First, we verify the scan chain correctness by inputting a test pattern and observing the output of the rightmost scan chain. If this operates correctly, the other identical modules are assumed to function properly. Second, we verify the correct DEP signals by using a metal line that connects an electrode to a transmission gate, which outputs the signal to an oscilloscope for observation.

These testability features comprehensively verify the chip's functionality. The first feature ensures the correct input of test patterns, while the second confirms the proper DEP signal output to the top metal layer. Once the waveform output was verified, experiments using polystyrene microparticles as cell mimics were conducted. A solution containing polystyrene microparticles is dispensed onto the surface of the chip, and their movement is observed through a microscope positioned above the chip.

Measurement results indicate that when the testing output is enabled, the maximum achievable DEP frequency is limited to 1 MHz due to large external loading, resulting in a voltage drop exceeding 10% [13]. This issue is resolved when the testing output is disabled, allowing the system to reach the maximum DEP frequency of 30 MHz, the limit of the function generator used in the setup. Table I compares this work with other programmable DEP systems. Our design has the smallest electrode size and smallest spacing between electrodes among related works. It operates at lower DEP voltages, covers a wider frequency range, and supports various waveforms. Additionally, our chip allows multiple experiments on a single sample, distinguishing it from existing solutions.

Reference	This Work	JSSC '03 [14]	LOC '08 [15]	TCASII '22 [21]	TBioCAS '23 [22]
Application	Cell Manipulation and Patterning	Cell Manipulation and Detection	Cells and Droplets Manipulation	Cell Sorting	Analyte Detection and Particle Manipulation
Method	nDEP	DEP Cage	pDEP	Traveling Wave DEP	DEP
Process / Technology	0.18 µm CMOS	0.35 µm CMOS	0.35 µm CMOS	0.18 µm 1P6M CMOS	0.13 µm BiCMOS
Chip Size	1.47 mm × 1.28 mm	8 mm × 8 mm	2.32 mm × 3.27 mm	3.2 mm × 2.2 mm	7 mm × 7 mm
Number of Electrodes	16,384 (128 × 128)	102,400 (320 × 320)	32,768 (128 × 256)	1,800 (30 × 60) 115,200 (240 × 480) (sub-)	4,096 (64 × 64)
Electrode Size	10 µm × 10 µm	20 μm × 20 μm	11 μm × 11 μm	52 μm × 52 μm 5 μm × 5 μm (sub-)	28 μm × 28 μm
Electrode Spacing	0.28 μm	-	0.6 µm	1.5 μm	22 µm
DEP Voltage	1.8 V	Max 5 V	Max 5 V	1.26 V	3 V
DEP Frequency	DC to 30 MHz	10 MHz	DC to 1.8 MHz	100 Hz to 20 MHz	1 kHz
Fluid Chamber Height	200 μm / without limit	85 µm	200 µm	50 µm	NA
Moving Speed	27 μm/s	10 µm/s	30 µm/s	1.5 μm/s	NA
Features	Low Voltage, Multiple Experiment on a single sample	Precise Individual Cell Manipulation	Droplet Manipulation	Traveling Wave DEP, Subelectrode Design	Functions Integration

TABLE I Comparison of DEP Chips



Fig. 10. Pattern design and corresponding separation ridges highlighted in red.(a) Separation ridges between phase-different electrodes form closed loops.(b) Intersection of separation ridges.

## E. Power Consumption

Temperature management is crucial in DEP systems because excessive heat can adversely affect cell viability. Operating at a low voltage of 1.8 V minimizes the risk of damaging cells due to high electric fields and results in low power consumption, thereby reducing thermal effects on the chip surface.

At a high clock frequency of 10 MHz, the chip's dynamic power consumption reaches 13.4 mW. However, this is not a practical operating mode for DEP manipulation, as the transition time would occupy 100% of the cycle, making particle manipulation ineffective. In practical operation, the power consumption is related to the pattern update rate. At a frame rate of 50 fps, the dynamic power consumption is measured at 136.7  $\mu$ W, and 8.45  $\mu$ W at 2 fps. Given these low power levels, the chip's surface temperature is not expected to rise significantly, ensuring a thermally safe environment for cell manipulation.

## IV. PATTERN DESIGN

# A. Pattern and Corresponding Separation Ridges

The generation of separation ridges only occurs between electrodes with different phase inputs and around the periphery of the electrode array. As a result, these separation ridges invariably form closed loops and cannot produce isolated line segments. For instance, in an  $8 \times 8$  electrode array as depicted in Fig. 10(a), assigning 6 electrodes on the left to a different phase aims to create a single line segment of separation ridges. However, this actually forms a closed separation ridge loop. Similarly, the  $3 \times 8$  electrodes on the right generate one major separation ridge and three weaker ones, yet still form a closed loop. The weaker separation ridges arise due to the non-uniform electric field in the regions between electrodes and the areas outside the electrode array where there are no electrodes. This inherent characteristic of forming closed loops complicates the design of patterns.

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## B. Design Considerations for Pattern Effectiveness

The example on the left side of Fig. 10(a), where 6 electrodes are assigned a different phase, results in two closely spaced separation ridges. This close proximity leads to mutual interference between the separation ridges, thereby diminishing the DEP force.

Similarly, when two separation ridges intersect, as depicted in Fig. 10(b), the close proximity at the intersection also causes mutual interference, further weakening the DEP force. Consequently, when designing patterns, it is crucial to minimize the number of intersections and maintain an adequate distance between separation ridges to achieve optimal results. Experimental results on the mutual interference between closely spaced separation ridges are discussed in the Experiment section.

#### C. Time-sharing Pattern

To reduce the complexity and crossover of separation ridges, we propose the 'time-sharing pattern' concept. This approach decomposes a complex pattern into multiple simpler patterns and alternates between them continuously. This method ensures that adjacent or intersecting separation ridges do not appear on the chip surface simultaneously, thereby reducing mutual interference.



Fig. 11. Various patterns used to divide particles into four groups. (a) Single separation ridge. (b) Single separation ridge in the X direction. (c) Double separation ridge in the X direction. (d) Time-sharing pattern.

Fig. 11(a) illustrates a fixed pattern where horizontal and vertical separation ridges intersect, causing interference that concentrates some particles at the intersection points. In contrast, Fig. 11(d) demonstrates a time-sharing pattern, decomposing the horizontal and vertical ridges from Fig. 11(a) into two separate patterns. Alternating between these two patterns results in a more effective result compared to using the fixed pattern alone.

#### V. EXPERIMENT RESULTS

#### A. Pattern Experiments

To investigate the behavior of particles under closely spaced or intersecting DEP separation ridges, we designed multiple patterns to separate particles into four groups, as shown in Fig. 11 and Fig. 12. The 2-second results were used to calculate the speed of particles within each pattern, while the 1-minute results indicate the steady-state distribution of the particles and the maximum range over which the pattern can affect particle movement. 20  $\mu$ m polystyrene particles were used in this experiment. The DEP force was generated by applying two 1 MHz sine wave signals with 1.8 V amplitude and a 180° phase difference.

1) Straightforward Pattern: The first pattern used a single line of electrodes with different phase selections to separate particles, as shown in Fig. 12(a). This straightforward design caused mutual interference between separation ridges at both edges of the line, weakening their strength. The 2-second result in Fig. 12(a) shows a notable reduction in particle velocity compared to Fig. 11(a), and the 1-minute result indicates a limited influence range for this pattern.

2) Refined Pattern: A more effective pattern used a single separation ridge, as shown in Fig. 11(a). This arrangement significantly increased the force on particles, resulting in a speed of 27  $\mu$ m/s and a maximum range of 120  $\mu$ m. However, particle accumulation was observed at the intersections of the separation ridges due to mutual interference.

3) Calculation of Moving Distance and Speed: The distance d particles moved due to a single separation ridge was determined by taking the half-width of the full separation width  $\alpha$  caused by the separation ridge, as illustrated in Fig. 13(a). For double separation ridges, the distance d was calculated by subtracting the distance between the separation ridges  $\beta$  from the total separation width  $\alpha$  and dividing by 2, as illustrated in Fig. 13(b). Similarly, the speed was defined as the aforementioned distance divided by 2 seconds. For example, the maximum speed achieved by the pattern in Fig. 11(a) was calculated by dividing the 2-second distance result d = 108µm by 2 and then dividing by 2 seconds, resulting in 27 µm/s.

4) Complexity and Interaction of Separation Ridges: Based on the results in Fig. 11(a), we determined that the effective distance of a single separation ridge was approximately 120  $\mu$ m. To further analyze the interaction between separation ridges, we tested patterns with spacings ranging from 10  $\mu$ m

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Fig. 12. Mutual interference of separation ridges at different spacings, with results shown for 2 seconds and 1 minute. Spacings are (a) 10  $\mu$ m, (b) 20  $\mu$ m, (c) 40  $\mu$ m, (d) 80  $\mu$ m, and (e) 160  $\mu$ m. Note that at 160  $\mu$ m, particles concentrate between the ridges due to the wide spacing.



Fig. 13. Method for calculating particle moving distance. (a) single separation ridge. (b) double separation ridges.

to 280  $\mu$ m. The results, shown in Fig. 14 and Fig. 15, indicate that closely spaced separation ridges experienced weakened forces due to mutual interference. As the spacing increased, the behavior gradually approached that of a single separation ridge. Specifically, separation ridges spaced more than 240  $\mu$ m apart exhibited performance similar to that of a single separation ridge.

5) *Time-sharing Pattern:* The single separation ridge result in Fig. 11(a) shows some particles accumulating at the center

where two separation ridges intersect. This issue can be resolved by using a time-sharing pattern shown in Fig. 11(d). Instead of having separation ridges crossing simultaneously, the time-sharing pattern ensures that only one separation ridge is active at any given time. When the designed pattern includes multiple closely spaced separation ridges, the time-sharing concept can also be employed to reduce the complexity of the electric field on the chip surface.

### B. Particle Patterning

This experiment demonstrates the chip's capability to arrange particles into predefined patterns. Before the experiment, 10  $\mu$ L of the polystyrene particle solution was applied to the chip. After one minute for particle sedimentation, a pattern resembling 'TBioCAS,' as shown in Fig. 17(a), was programmed into the chip. The resulting particle arrangement, shown in Fig. 16(b), was observed 30 s after programming the pattern, demonstrating that DEP forces effectively repelled particles from the designated areas, creating a particle-free 'TBioCAS' pattern. This capability extends to programming various particle arrangements on the chip, demonstrating potential applications in configuring cells into specific shapes or patterns.

# C. Concentration Control for Experimental Requirements

Concentration control is an essential step in most cell experiments as it ensures experimental consistency and reliability.



Fig. 14. Effect of different distances between separation ridges on the distance traveled by particles.



Fig. 15. Effect of different distances between separation ridges on particle speed.

To increase concentration, particles were focused using a series of patterns, as in Fig. 17(c). To obtain specific dilution factors (e.g., 1/1024), an iterative dilution process was implemented.

Initially, particles on 1/4 of the chip area were fixed in place, while the remaining particles were removed using a sequential pattern illustrated in Fig. 17(b). The corresponding result is shown in Fig. 16(c). Following this, particles were separated using the time-sharing pattern illustrated in Fig. 11(d) and then focused on the centers of four quadrants using the pattern sequence illustrated in Fig. 17(c), with the corresponding result displayed in Fig. 16(d). Subsequently, the particles were divided into 16 groups using a time-sharing pattern illustrated in Fig. 17(d) and (e) with the corresponding result shown in 16(e). After that, the outer 12 groups of particles were eliminated using the pattern sequence shown in Fig. 17(b). This sequence of processes, from Fig. 17(b) to (e), resulted in a 1/4 reduction of particles on the chip surface per iteration, achieving a 1/1024 dilution after five iterations. Alternatively, dilutions of arbitrary ratios can also be achieved. Finally, the particles were evenly dispersed using a randomly generated pattern, thus completing the dilution process, as shown in Fig. 16(g).

#### D. Single Particle Manipulation

Single particle manipulation is crucial as it allows the precise removal of low-quality cells, ensuring space and resources for high-quality ones. To achieve this, we used YOLOv8, an object detection algorithm [23], to identify and locate 20 µm polystyrene particles. YOLOv8's real-time detection capabilities enabled dynamic tracking of particle positions. Based on the identified positions, a series of DEP patterns were generated and programmed into the chip to guide the particles toward the corners or off the chip surface. This method effectively isolated or removed unwanted particles.

## E. Multiple Experiments on a Single Sample

The above experiments, including particle patterning, concentration control, and single-cell manipulation, are conducted sequentially on the same chip without changing the sample. This capability sets our chip apart from traditional DEP chips, which generally perform a single task and require chip replacement for different experiments, potentially introducing human interference and contamination. Our chip's ability to adjust concentration before each experiment ensures consistent conditions, regardless of initial sample concentration. This feature is crucial, as different experiments require varying concentrations: high concentrations for particle patterning to ensure effective aggregation, and low concentrations for single particle manipulation to prevent particle overlapping. By enabling multiple experiments on a single sample with adjustable concentrations, our chip offers a more streamlined approach to cell-based research. The full video of the experiment in Fig. 16 is available at: https://dx.doi.org/10.21227/8v4r-2549 [24].

#### F. Cell Experiments

iPSCs can differentiate into any cell type, making them valuable in regenerative medicine. However, their production is labor-intensive and relies on manual control, limiting scalability and introducing variability that restricts their therapeutic potential. To address these challenges, standardized automated production processes and increased manufacturing volumes are needed [25].

Since the size of iPSC aggregates influences differentiation outcomes [3]–[5], we conducted a prototype experiment on aggregation control. This demonstrates our chip's capability to provide programmable patterns for desired aggregations and allows multiple aggregation experiments on a single platform. This approach could streamline the manufacturing workflow and contribute to the standardization of iPSC mass production



Fig. 16. Multiple experiments on a single sample. (a) High-concentration particles. (b) Result of the 'TBioCAS' pattern. (c) Result of the pattern sequence that removes excess particles. (d) to (g) Dilute particles on the chip using the pattern sequence in Fig. 17(b) to (e). (g) and (h) Single particle manipulation.



Fig. 17. Patterns for the 'multiple experiments on a single sample' experiment. (a) 'TBioCAS' pattern. (b) Pattern sequence that removes excess particles. (c) Pattern sequence that moves particles to the center of four quadrants. (d) and (e) Time-sharing pattern to divide particles into 16 groups. (f) Pattern sequence for single particle manipulation.

1) *iPSC Aggregation Control:* Conventional methods for controlling aggregation size , such as AggreWell<sup>TM</sup> are limited to producing only one aggregation size at a time. In contrast, our chip uses programmable patterns to control desired aggregations, allowing for multiple aggregation experiments on a single chip. Before starting the experiment, an enzyme solution was added to return the cells to a single-cell state. A 10  $\mu$ L sample was then applied to the chip, and after 2 minutes for the cell sedimentation, the predefined time-sharing pattern was input into the chip. Fig. 18(a) shows the pattern used, and Fig. 18(b) is a snapshot taken 1 minute after the pattern was applied.



Fig. 18. iPSC aggregation with different sizes on the proposed chip. (a) The time-sharing pattern used in the experiment. (b) Result after 1 minute of manipulation.

2) *iPSC Viability Post-Manipulation:* We assessed the viability of *iPSCs* following DEP manipulation under five different conditions: stored in an Eppendorf tube at room temperature (RT), placed on the chip without manipulation (OC), and manipulated on the chip for 1 minute, 5 minutes, and 10 minutes. To ensure constant DEP forces acting on the *iPSCs* during the experiment, we used four patterns shown in Fig. 19, which rotated in order, changing every minute. Cell viability was evaluated using Trypan Blue and the CellDrop BF Automated Cell Counter. The results, shown in Fig. 20, indicate similar viability rates across all conditions, suggesting that the DEP system does not affect cell viability during the duration of the experiment.

3) Challenges and Future Directions: Our DEP system has previously demonstrated the ability to manipulate various cell types, including THP-1 cells and fibroblasts, as presented

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Fig. 19. Four patterns used to continuously move iPSCs before conducting viability evaluation. Patterns (a), (b), (c), and (d) rotate every minute. The background images show the distribution of iPSCs after being moved.



Fig. 20. Cell viability results under different conditions. RT: cells stored in tubes at room temperature. OC: cells on the chip system without manipulation. 1 min: cells manipulated for 1 minute. 5 min: cells manipulated for 5 minutes. 10 min: cells manipulated for 10 minutes.

in [13]. This capability extends to testing conditions with phosphate-buffered saline (PBS), and we are currently evaluating additional cell types. While our system shows versatility, cells that tend to adhere to surfaces may not move efficiently on our chip.

This paper highlights the flexibility of our system in manipulating cell aggregation sizes, dilution, and patterning, which opens possibilities for biotechnology applications requiring precise cell handling, including quantitative sample dilution, controlled cell assembly, studies of cell-cell interaction, and patterned cell cultures. Although further steps such as harvesting clusters or integrating this technology into a complete workflow depend on specific applications, future work could explore methods for post-manipulation processing.

#### VI. CONCLUSION

This paper presents a programmable CMOS DEP chip with a  $128 \times 128$  array of individually addressable 10 µm microelectrodes. Operating at a low voltage of 1.8 V, the chip achieves particle manipulation speeds of up to 27 µm/s while maintaining cell viability. The chip's reconfigurable nature allows for sequential experiments on the same chip and sample, demonstrated through particle patterning, concentration control, and single-particle manipulation. This versatility reduces manual intervention and contamination risks associated with traditional single-function DEP chips. The innovative time-sharing pattern approach mitigates mutual interference between separation ridges, enhancing overall manipulation efficiency. Future work will integrate capacitive sensors for real-time feedback on cell quality and position, and enhance system automation for more complex and large-scale biological experiments. In summary, the programmable CMOS DEP chip represents a significant advancement in cell manipulation, offering a flexible, low-voltage, and biocompatible solution for non-invasive cell handling.

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