Lin-Hung Lai
(Henry)

Digital IC & Biochip Designer

CONTACT

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EDUCATION

Statistics (Visiting PhD)
Stanford University
Wong Lab instituted by Wing Hong Wong
2025 - 2026 (Expected)

Electronics Engineering (PhD)
National Yang Ming Chiao Tung University
NYCU, Si2 Lab instituted by Chen-Yi Lee
2021 - 2025 , GPA 4.3/4.3

Electronics and Computer Engineering (BS)
National Chiao Tung University
2017 - 2021, Rank: 1/50

SKILLS

IC, Hardware Design & Verification

- Verilog, SystemVerilog
- Hspice, Virtuoso

EDA Tools

- Design Compiler, VCS, Verdi
- Innovus, PrimeTime, Jaspergold

Software Development

- C++, C, Python
- Shell Script, HTML

System Integration

- FPGA, Vivado
- Raspberry Pi, Arduino
- PCB

AWARDS

Bronze Medal Award, 2025
Macronix Golden Silicon Awards

NYCU Student Affairs Office, 2024
Distinguished Contribution Award

Scholastic Honor Society Awards, 2025
Phi Tau Phi Awards

1st Prize Award, 2021
TSMC Intern Final Competition

EXPERIENCE

Project Leader Jan. 2021 - Apr. 2025

System Integration & Silicon Implementation Lab, NYCU

- Led 7 chip tape-outs, 6 IEEE papers, and 2 patents across TW/US/JP
- Built a CMOS capacitive sensor system to capture high-res cell images using multi-sampling and pixel-wise data fusion
- Managed 10+ graduate students, drove collaboration with CiRA Foundation and TVGH, and won the 2023 Taipei Biotech Award

Sr. Teaching Assistant 2021 Spr, 2021 Fal, 2023 Fal

Integrated Circuit Design Lab, NYCU

- Guided 300+ students across RTL to Layout projects; supervised 14 digital IC projects, including Low Power / CDC / STA / Verification etc
- Led 12 TAs in course delivery and debugging Verilog / SystemVerilog ASIC projects, awarded 2024 Prominent TA, 2023 Outstanding TA

Hardware Engineer Intern Jul. 2021 - Aug. 2021

Division of System and Chip Design Solutions, TSMC

- Built a 3DIC BGA optimizer (C++ / Python) for early-stage signal and power integrity planning in cell-based CAD flow
- Improved routing quality by 30%, won 1st place out of 100+ interns

Lecturer of Logic Synthesis 2024 Summer

Taiwan Semiconductor Research Institute, TSRI

PROJECTS

ProDEP: Silicon-Defined Digital Control of Living Cells

Capstone Research Project

- Enabled real-time single-cell manipulation using a full-custom CMOS chip (128×128 electrodes), integrated with FPGA, WiFi-RPi interface, Python GUI and optical feedback portable system
- Demonstrated full-stack silicon-to-system ownership, leading to startup spin-off (CyensTech, NT$7.2M funding)

CDC-Proven FIFO on 16nm FinFET – From RTL to APR

Integrated Circuit Design Laboratory Project

- Built an async FIFO using gray code and handshake synchronizers, solving multi-clock domain issues with formal check (JasperGold).
- Implemented on TSMC 16nm ADFP, integrating clock gating, 2-port SRAM, and full RTL→APR flow with power/timing analysis
- Gained hands-on experience solving metastability, process scaling

16-bit RISC CPU with AXI and Cache Optimization

Integrated Circuit Design Laboratory Project

- Built a 5-stage pipelined 16-bit CPU with AXI protocol and separate I/D cache to reduce memory latency
- Applied multi-stage multiplier to balance cycle time and timing closure

Floating-Point CNN Accelerator for Similarity Matching

Integrated Circuit Design Laboratory Project

- Designed CNN accelerator with convolution, pooling, FC, activation
- Integrated IEEE-754 datapath using DesignWare FP IP
- Tuned for low latency and area efficiency