Lin-Hung Lai Curriculum Vitae

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Research Statement

With 5 years in Bio-IC design, specializing in cell-related sensors and actuators like capacitive sensing arrays (CSA) and dielectrophoresis (DEP) CMOS biochips. Possesses solid knowledge in semiconductor design methodology and biological applications. Expertise in developing digital architectures and integrating custom ICs with optical platforms, FPGAs, and PCs for comprehensive data analysis, combined with strong software development skills. Gained 3DIC and FinFET experience through a TSMC internship and 4 years as a lecturer/TA. Currently seeking to optimize at the algorithm level using cross-disciplinary expertise in semiconductors, biomedical chips, and computational biology.

Education

2025.04-2026.01 **Visiting Ph.D. Student** - Stanford University, Stanford, CA, U.S.
Department of Statistics (Advisor: Prof. Wing Hung Wong)

2021.02-2025.03 **Ph.D. Student** - National Yang Ming Chiao Tung University, Hsinchu, Taiwan
Institute of Electronics Engineering (Advisor: Prof. Chen-Yi Lee, GPA: 4.3)
Dissertation: Super-Resolution Capacitive Imaging Array and Programmable Cell Manipulation Biochip: Design, Integration and Optimization

2017.09-2021.01 **Bachelor of Science** - National Chiao Tung University, Hsinchu, Taiwan
Department of Electronics and Computer Engineering (GPA 4.27, Rank 1/50)

Professional Experience

2025.04-2026.01 **Visiting Student Researcher** - Stanford University, CA, U.S.
Wong Lab @ Stanford Bio-X (Advisor: Prof. Wing Hung Wong)

- Executed end-to-end experimental validation of cell manipulation on chip, combining electrode control, live-cell handling, and system-level integration across hardware and wet-lab domains
- Developed a scalable, collision-free RL-based routing algorithm for 128×128 DEP Bio CMOS chips

2021.02-2025.03 **Research Project Leader** - National Yang Ming Chiao Tung University, Hsinchu, Taiwan
System Integration & Silicon Implementation Lab (Advisor: Prof. Chen-Yi Lee)

- Directed and managed the tape-out of 7 chips and oversaw the publication of 6 papers and 2 patents, coordinating with 10+ master and PhD students, resulting in strengthening research collaborations with institutions like the CiRA foundation, TVGH Hospital and NYCU regenerative medicine center.

2022.07-2022.07 **Visiting Scholar** - Kyoto University, Kyoto, Japan
Center for iPS Cell Research and Application Foundation (CiRA_F)

- Investigated cutting-edge techniques and instrumentation for stem cell quality assessment
- Conceptualized forward-looking chip designs aligned with rigorous biomedical standards

2021.07-2021.09 **Summer Intern** - Taiwan Semiconductor Manufacturing Company (TSMC), Hsinchu, Taiwan
System and Chip Design Solutions Development Division (3D IC, BGA Optimization)

- Developed a CAD tool with C++ and Python that optimizes 3D IC BGA assignments and fast routing to enhance power and signal integrity in early stages
- Achieved 1st place in TSMC Intern Final Competition, demonstrating problem-solving expertise.

2023.01-2025.03 **Senior IT/Server Manager** - National Yang Ming Chiao Tung University, Hsinchu, Taiwan
Institute of Electronics Engineering (30+ HPC Server, IP/DNS/Network)

Technical Skills

Hardware Design: Verilog, System Verilog, VHDL, Layout(mixed-signal), 7 chips tape-out and measurements
Software Design: Python, C, C++, Shell Script, HTML, MATLAB
EDA Tools: Irun, VCS, Verdi, Design Compiler, Innovus, PrimeTime, Jaspergold, Hspice, Virtuoso
System Integration: GUI, FPGA, Arduino, Raspberry Pi, PCB, Microfluidic

Honors and Awards

2024.09 **Prominent Teaching Assistant Award**, Academic Affairs Office, NYCU (Top 6 awardees university-wide)
2024.05 **Best Paper on Sensory Systems Award**, IEEE International Symposium on Circuits and Systems
2024.04 **Young College Elite Award**, Hsinchu City Government
2024.03 **Distinguish Contribution Award**, National Yang Ming Chiao Tung University
2024.03 **Graduate Student Award**, College of Electrical and Computer Engineering, NYCU
2023.05 **Interdisciplinary Taipei Biotech Award**, Taipei City Government
2023.10 **Outstanding Teaching Assistant Award**, Academic Affairs Office, NYCU
2021.07 **1st Place in TSMC**, TSMC Intern Competition (over 100 peers)
2018-2021 **Academic Excellence Award for 4 Times**, Dept. of Electronics and Computer Engineering, NYCU
2016.12 **Silver Medal Award in Physics**, Macronix Science Awards

Personal Fellowship

2025--2026 **Ph.D. Students Study Abroad Fellowship**, National Science and Technology Council, NSTC ($22,500)
2021--2025 **Ph.D. Fellowship**, Taiwan Semiconductor Manufacturing Company, TSMC ($80,000)
2019--2024 **Distinguished Students Fellowship**, Hshin Tian Kong ($18,000)
2022 **Visiting Student Fellowship**, CiRA Foundation ($1,000)
2021--2022 **Freshman Ph.D. Fellowship**, Institute of Electronics ($6,400)
2020 **Undergraduate Research Fellowship**, Ministry of Science and Technology, MOST ($1,600)
2019--2022 **Distinguished ECE Student Fellowship**, Hsiao Yuan Lung Scholarship ($1,200)
2018--2019 **Pan Wan Yuan Fellowship**, Pan Wan Yuan Foundation ($1,600)
2017--2020 **Silver Medal Award Fellowship**, Macronix Science Awards ($6,600)

Teaching Experience

2024 Summer **Lecturer**: Logic Synthesis with ADFP (TSMC N16 FinFET Technology)
Taiwan Semiconductor Research Institute (TSRI)
Teaching Assistant: Physical Design with ADFP
Taiwan Semiconductor Research Institute (TSRI)

- Lectured / Lab on topics related to IC design techniques using ADFP to about 30 European students

2024 Spring **Lecturer**, Asynchronous FIFO Design in 16nm FinFET Technology
Institute of Electronics, NYCU

2023 Fall **Senior Teaching Assistant**, EEIE30041: Integrated Circuit Design Lab
Institute of Electronics, NYCU

- Lead a team of 7 TAs through an extensive digital IC design course covering 14 topics/projects, from RTL to layout level. Approximately 160 graduated students
- Expert in the implementation of optimization techniques for performance, area, and power efficiency. Received the 2023 Outstanding Teaching Assistant Award

2022 Fall **Senior Teaching Assistant**, EEEC20004: VLSI Lab
Department of Electronics and Computer Engineering, NYCU

- Lecture covered top-down design flow, standard cell library, and full-custom layout approaches, emphasizing performance, area, and power optimization.

Senior Teaching Assistant, EEEC20004: Introduction to VLSI Design
Department of Electronics and Computer Engineering, NYCU

- Host TA time, and assisted the professor with post-lecture explanations for a VLSI Design.

2021 Fall **Senior Teaching Assistant**, EEIE30041: Integrated Circuit Design Lab
Institute of Electronics, NYCU

2021 Spring **Teaching Assistant**, EEIE30041: Integrated Circuit Design Lab
Institute of Electronics, NYCU

Publications and Patents

Journal Papers

1. **Lin-Hung Lai**, Wen-Yue Lin, Yu-Chen Hung, and Chen-Yi Lee. "Super Resolution Capacitive Sensor Array with Adaptive Fusion Pixel for Multiscale iPSC Spheroid Analysis." ***IEEE Sensors Journal***, submitted January 13, 2025 (Under Review).

2. Wen-Yue Lin, **Lin-Hung Lai**, Yi-Wei Lin, and Chen-Yi Lee. "A Programmable CMOS DEP Chip for Cell Manipulation." ***IEEE Trans. Biomed. Circuits Syst.***, 2024.

3. **Lin-Hung Lai**, Wen-Yue Lin, Yu-Wei Lu, Heng-Yu Lui, Shinsuke Yoshida, Shih-Hwa Chiou, and Chen-Yi Lee. "A 460,800 Pixels CMOS Capacitive Sensor Array With Programmable Fusion Pixels and Noise Canceling for Life Science Applications." ***IEEE Trans. Circuits Syst. II: Express Briefs***, vol. 70, no. 5, pp. 1734–1738, 2023.

Conference Papers

1. Dun-You Li, **Lin-Hung Lai**, Wen-Yue Lin, and Chen-Yi Lee. "F*: Synchronous, and Collision-Aware Multi-Cell Routing on DEP Biochips for Efficient Cell Transportation." Submitted to ***IEEE/ACM ICCAD***, 2025 (Under Review).

2. **Lin-Hung Lai**, Wen-Yue Lin, Yu-Chen Hung, Yu-Hsian Wang, Hsi-Hao Huang, and Chen-Yi Lee. "Multiple Sampling and Pixel-Wise Accumulation in CMOS Capacitive Sensor Array System for Real-Time Droplet Analysis." ***IEEE ISCAS***, London, 2025.

3. Yu-Hsiang Wang, Wen-Yue Lin, **Lin-Hung Lai**, and Chen-Yi Lee. "Smart Pattern Generation on Programmable Dielectrophoresis Array Chip for Single Particle Manipulation." ***IEEE ISCAS***, London, 2025.

4. Wen-Yue Lin, **Lin-Hung Lai**, Yi-Wei Lin, and Chen-Yi Lee. "A Programmable CMOS Dielectrophoresis Array Chip with 128×128 Electrodes for Cell Manipulation." ***IEEE ISCAS***, Singapore, 2024, pp. 1–5.

5. Heng-Yu Liu, **Lin-Hung Lai**, Wen-Yue Lin, Yu-Wei Lu, Yi-Wei Lin, and Chen-Yi Lee. "A 2.56-µs Dynamic Range, 31.25-ps Resolution 2-D Vernier Digital-to-Time Converter (DTC) for Cell-Monitoring." ***IEEE ISCAS***, Singapore, 2024, pp. 1–5. doi:10.1109/ISCAS58744.2024.10558438.

Patents

1. C.-Y. Lee, **Lin-Hung Lai**, W.-Y. Lin. "Capacitance Sensor Array Chip with Programmable Fusion Pixels, Sampling Device Thereof and Controlling System Thereof." **U.S. Patent** Application No. 18/668,308 (Filed: May 20, 2024, Under Review). Also filed as **Taiwan Patent** No. 113118659 (issued), **Japan Patent** No. 2024-081458.

2. C.-Y. Lee, W.-Y. Lin, **Lin-Hung Lai**. "Programmable Dielectrophoretic Semiconductor Chip, Packaging Structure and Control System Thereof." **U.S. Patent** Application No. 18/762,720 (Filed: July 3, 2024, Under Review). Also filed as **Taiwan Patent** No. 113124980, **Japan Patent** No. 2024-107133.

Highlighted Projects

2022.04-2025.04 **NSTC #113-2321-B-A49-009** Total fund: $1,230,000 Role: Sub-Project Leader
Title: Innovative Induced Pluripotent Stem Cells Validation Biomedical Chips and Precision Regeneration Platform for Preclinical Evaluation.

- Led the design and development of an automated monitoring and quality control system for stem cells using CMOS technology and DEP, improving precision and efficiency in stem cell evaluation.
- Pioneered the flexible design of single-cell resolution capacitive sensing arrays and integrated them into the bio-system, enhancing the system's versatility and application in biomedical research.

2024.07-2025.07 **MOE #1132702835C** Total fund: $750,000 Role: Sub-Project Leader
Title: Advanced Process IC Design Environment Development Program.

2022.06- **TSMC JDP** Total fund: $80,000 Role: Project Leader
2023.06 Title: ADFP FinFET Design Education Booster.

Invited Talks

2024.12 ICLAB Special Lecture, NYCU, Hsinchu, Taiwan (Invited speaker on advanced digital IC design: CPU architecture, FinFET, and 3D IC technologies)
2024.10 AICD Workshop on Server Deployment and Cybersecurity for Advanced IC Design, AJ Hotel, Hsinchu, Taiwan (Invited speaker on secure server infrastructure and system administration for IC design labs)
2024.08 AICD Advanced IC Design Environment Forum, National Taiwan University, Taipei, Taiwan
2023.01 ICLAB Special Lecture, NYCU, Hsinchu, Taiwan (Invited speaker on advanced digital IC design: CPU architecture, FinFET, and 3D IC technologies)

Leadership and Service

2023--2024 **Chair** - NYCU Student Representative Council, Responsible for organizing council meetings, decision-making, and liaising with the school administration and other student organizations
2022--2025 **Student Representative** - College of Electrical and Computer Engineering, in charge of the Curriculum Committee and participation in college affairs meetings
2021--2022 **Member** - IEEE Eta Kappa Nu (HKN), the International Honor Society, contributing to academic excellence and professional growth through leadership and service
2018--2021 **Vice President** - Union of MXIC Science Awards, fostering a collaborative network of over 500 alumni to promote continuous innovation and professional exchange in science and technology